REMARKS

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicant asserts that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

Status of Claims

Claims 1-19 are pending in the application. Claims 1-19 have been rejected.

CLAIM REJECTIONS

35 U.S.C. § 102 Rejections

In the Office Action, the Examiner rejected claims 1-6, 9-16 and 19 under 35 U.S.C. § 102(b), as being anticipated by Roohparvar (U.S. Patent No. 6,529,417). Applicant respectfully traverses the rejection of claims due to the fact that the cited reference neither teaches nor suggests all the limitations recited in independent claims 1, 9 and 19 as previously presented. More specifically, all the pending independent claims included the limitation of an **erase pulse** having a **predominantly non-flat** and **non-linear** voltage profile, where as the cited reference teaches an **erase voltage profile** which is defined throughout the specification as being **ramped**. By definition, a ramped voltage is predominantly linear. The dictionary definition of a ramp generator is:

> ('ramp 'jen·ə'rād·ər) A circuit that generates a sweep voltage which **increases linearly** in value during one cycle of sweep, then returns to zero suddenly to start the next cycle.

Applicant believes the source of the Examiner's confusion may stem from the fact that the ramp shown in the figures associated with a digital embodiment of the cited reference show a ramp produced by a set of constituent **flat** steps. Nevertheless, the predominant and intended

characteristic of the erase voltage profile is that of a **ramp**. The cited reference elaborates and confirms this assertion throughout the specification, including:

> "..The ramped erase voltage signal is then applied to sources of the memory cells during an erase operation. Both analog and digital circuits are described for generating the **ramped** reference voltage signal." [Abstract]
>
> "By **ramping** the voltage applied to the source, the invention allows electron tunneling to occur while reducing the current through the floating gate oxide layer.... The memory also comprises a source regulation circuit for applying a **ramped voltage signal** to sources of the floating gate memory cell transistors during an erase operation..... A **voltage ramp generator is provided** which has an output connected to the second input of the differential amplifier for providing a ramped reference voltage signal. An output circuit is connected to the output of the differential amplifier for providing a **ramped voltage signal** to be coupled to sources of the floating gate memory cell transistors during an erase operation.... The method comprises the steps of coupling a control gate of the memory cell to a low voltage potential, **generating a pulsed ramped voltage signal**, and applying the pulsed ramped voltage signal to a source of the memory cell. [Summary]

Since the relied upon prior art teaches exclusively teaches the use of a **ramped voltage**, be it generated with an analog source or a digital source with uses steps, and a **ramped voltage** by definition has a predominantly **linear voltage profile**, the cited reference is missing a key limitation of the pending independent claims.

As is well established, in order to successfully assert a prima facie case of anticipation, the Examiner must provide a single prior art document that includes every element and limitation of the claim or claims being rejected. Applicant respectfully asserts that the cited reference is not sufficient as a single prior art document for the purpose of establishing a prima facie case of anticipation. The cited reference neither teaches nor suggests every element and limitation of independent claims 1, 9 and 19, namely an erase pulse with a **predominantly non-flat and non-linear voltage profile**. Moreover, as shown above, the cited reference actually teaches away from the recited limitation of pending independent claims 1, 9 and 19.

Independent claims 1, 9 and 19 as clarified are considered allowable in view of the cited prior art. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the 102 rejections of independent claims 1, 9 and 19 and all claims dependent upon them.

35 U.S.C. § 103 Rejections

In the Office Action, the Examiner rejected claims 7, 8, 17 and 18 under 35 U.S.C. § 103(a), as being unpatentable over Roohparvar as applied to claims 6 and 16, and in view of Chindalore et al., U.S. Patent No. 6,839,280 B1.

In view of the remarks and arguments above regarding the 102 rejections, Applicant respectfully asserts that these claims are allowable by virtue of their dependence on allowable base claims. Reconsideration and withdrawal of the 103 rejections is respectfully requested.

In view of the foregoing amendments and remarks, all the pending claims are considered to be allowable. Their favorable reconsideration and allowance is respectfully requested.

Should the Examiner have any question or comment as to the form, content or entry of this Amendment, the Examiner is requested to contact the undersigned at the telephone number below. Similarly, if there are any further issues yet to be resolved to advance the prosecution of this application to issue, the Examiner is requested to telephone the undersigned counsel.

Please charge any fees associated with this paper to deposit account No. 50-3400.

Respectfully submitted,

Vladimir Sherman
Attorney for Applicant(s)
Registration No. 43,116

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